WHAT IS CLAIMED IS:

1. A computer system having a common display memory and main memory, comprising:

a display means;

a first plurality of internal and external memory subsystems;

a second plurality of memory channels;

a memory channel data switch and controller unit for allocating the memory channels among a plurality of subsystems;

a central processing unit (CPU) subsystem controller unit producing output signals to be applied to the memory channel data switch and controller unit;

a graphics/drawing and display subsystem producing output signals to be applied to the memory channel data switch and controller unit;

an arbitration and control unit producing output signals to be applied to the CPU subsystem controller unit and to the graphics/drawing and display subsystem;

a peripheral bus control unit producing output signals to be applied to the memory channel data switch and controller unit and to the arbitration and control unit; and

a direct input/output (I/O) control unit producing output signals to be applied to the memory channel data switch and controller unit and to the arbitration and control unit.

2. The computer system of claim 1 further comprising multiplexer means for muliplexing said external memory subsystems into at least one memory channel.

3. The computer system of claim 1 wherein one of said memory subsystems is a display memory which can also function as a main system memory.

4. The computer system of claim 1 wherein at least one of said memory subsystems includes a data manipulator containing a plurality of storage elements.

5. The computer system of claim 1 wherein said graphics/drawing subsystem can draw directly into any area of said main memory.

6. The computer system of claim 1 wherein said peripheral bus can transfer data into said main memory, and said graphics/drawing and display subsystem can utilize display refresh data without storing a copy of the display refresh data and without using a CPU.

7. The computer system of claim 1 further comprising a partial drawing buffer where a graphics engine can write a portion of the display output data and transfer the portion of the display output data to a common memory subsystem for use during subsequent display updates after a display frame has been processed.

8. The computer system of claim 1 further comprising a complete drawing buffer where a graphics engine can store the complete display output data and transfer the display output data for subsequent display updates.

9. The computer system of claim 1 further comprising:

a graphics controller for performing 3-D graphics functions; and

a texture cache from which the graphics controller can fetch data.

10. The computer system of claim 1 further comprising:

separate controllers for each memory subsystem;

an arbiter that takes requests from multiple subsystems; and

a memory data path through which a memory subsystem can provide memory data to a subsystem without preventing other subsystems from accessing other memory subsystems.

11. The computer system of claim 1 further comprising:

at least one graphics engine; and

at least one partial drawing buffer into which said at least one graphics engine can write a portion of display output data and transfer the portion of display output data for subsequent display updates.

12. The computer system of claim 1 further comprising:

a graphics controller for performing 3-D graphics functions; and

an order buffer from which said graphics controller can fetch data.

13. A computer system having a common display memory and main memory, comprising:

a display means;

a first plurality of internal and external memory subsystems;

a second plurality of memory channels;

a memory channel data switch and controller unit for allocating the memory channels among a plurality of subsystems;

a central processing unit (CPU) subsystem controller unit producing output signals to be applied to the memory channel data switch and controller unit;

a graphics/drawing and display subsystem producing output signals to be applied to the memory channel data switch and controller unit;

an arbitration and control unit producing output signals to be applied to the CPU subsystem controller unit and to the graphics/drawing and display subsystem; and

a peripheral bus control unit producing output signals to be applied to the memory channel data switch and controller unit and to the arbitration and control unit.

14. The computer system of claim 13 further comprising multiplexer means for muliplexing said external memory subsystems into at least one memory channel.

15. The computer system of claim 13 wherein one of said memory subsystems is a display memory which can also function as a main system memory.

16. The computer system of claim 13 wherein at least one of said memory subsystems includes a data manipulator containing a plurality of storage elements.

17. The computer system of claim 13 further comprising a complete drawing buffer where a graphics engine can store the complete display output data and transfer the display output data for subsequent display updates.

18. The computer system of claim 13 further comprising:

a graphics controller for performing 3-D graphics functions; and

a texture cache from which the graphics controller can fetch data.

19. The computer system of claim 13 further comprising:

separate controllers for each memory subsystem;

an arbiter that takes requests from multiple subsystems; and

a memory data path through which a memory subsystem can provide memory data to a subsystem without preventing other subsystems from accessing other memory subsystems.

20. The computer system of claim 13 further comprising:

a graphics controller for performing 3-D graphics functions; and

an order buffer from which said graphics controller can fetch data.

21. The computer system of claim 13 further comprising:

separate controls for each memory subsystem;

an arbiter that takes requests from multiple processor or peripheral subsystems; and

a memory data path wherein memory data can be provided by a memory subsystem to a processor or peripheral subsystem without preventing additional processor or peripheral subsystems from accessing other memory subsystems.

22. The computer system of claim 13 further comprising:

an integrated processor that receives input data from the memory channel data switch and controller unit and that provides output data to an input of the arbitration and control unit.

23. A computer system having a common display memory and main memory, comprising:

a display means;

a plurality of internal and external memory subsystems, each having its own memory channel;

a memory channel data switch and controller unit wherein the memory channels can be allocated to a plurality of processor or peripheral subsystems;

a CPU subsystem controller unit producing output signals received proportionally by the memory channel data switch and controller unit; and

an arbitration and control unit producing output signals received proportionally by the CPU subsystem controller unit.

24. An computer system having a plurality of internal and external memory subsystems comprising:

multiple concurrent memory channels;

a memory channel data switch and controller unit wherein the memory channels can be allocated to a plurality of processor or peripheral subsystems;

a means for a plurality of processors and peripheral subsystems to access the common memory regions; and

at least one of the internal memory subsystems is DRAM memory.

25. The computer system of claim 24 further comprising:

a multi-bank internal DRAM memory;

a means for multiple processor or peripheral subsystems to access a plurality of the banks; and

a means for an arbiter to allow multiple processor or peripheral subsystems to serially access a given bank of memory.

26. The computer system of claim 24 further comprising:

a bank of internal DRAM memory with multiple row buffers;

a means for multiple processor or peripheral subsystems to access a plurality of the row buffers; and

a means for an arbiter to allow multiple processor or peripheral subsystems to serially access a given row buffer.

27. A monolithic integrated circuit comprising:

at least one internal memory subsystem of DRAM memory;

at least one external memory control for DRAM memory;

a plurality of concurrent memory channels; and

a means for multiple compute engines, multiple processors or peripheral subsystems to access the memory channels;

28. The monolithic integrated circuit of claim 27 where multiple compute engines concurrently access said internal memory subsystem of DRAM memory through a data switch to a plurality of banks of memory.

29. The monolithic integrated circuit of claim 27 where a plurality of compute engines concurrently access said internal memory subsystem of DRAM memory through a data switch to a plurality of row buffers.

30. The monolithic integrated circuit of claim 27 where at least one of the said internal memory subsystems of DRAM memory includes a data manipulator containing a plurality of storage elements as well as a simple Arithmetic Logic Unit (ALU).

31. A computer system having a common display memory and main memory, comprising:

a display means;

a plurality of internal and external memory subsystems;

a central processing unit (CPU) subsystem controller unit producing output signals;

a graphics/drawing and display subsystem producing output signals;

an arbitration and control unit producing output signals to be applied to the CPU subsystem controller unit and to the graphics/drawing and display subsystem; and

a peripheral bus control unit producing output signals to be applied to the CPU controller unit and to the arbitration and control unit.

32. The computer system of claim 31 further comprising:

a graphics controller for performing 3-D graphics functions; and

a texture cache from which the graphics controller can fetch data.

33. The computer system of claim 31 further comprising:

a graphics controller for performing 3-D graphics functions; and

an order buffer from which said graphics controller can fetch data.